REMARKS

In the last Office Action, the Examiner objected to the abstract as not being in compliance with MPEP §608.01(b). Claims 1 and 7 were objected to as containing informalities. Claims 1, 2 and 7-9 were rejected under 35 U.S.C. §102(e) as being anticipated by U.S. Patent Application Publication No. 2003/0155943 to Morishita. Additional art was cited of interest.

In accordance with the present response, the specification has been suitably revised to correct informalities, provide antecedent basis for the claim language, conform to the drawing revisions, and to bring it into better conformance with U.S. practice. The title of the invention has been changed to "SEMICONDUCTOR DEVICE AND ELECTRONIC DEVICE EQUIPPED WITH SEMICONDUCTOR DEVICE" to more clearly reflect the invention to which the amended and new claims are directed. A new, more descriptive abstract in compliance with MPEP §608.01(b) has been substituted for the original abstract.

Original independent claims 1 and 7 have been amended to further patentably distinguish from the prior art of record and overcome the Examiner's objections. Original claims 1, 2 and 7-9 have also been amended in formal respects to improve the wording and bring them into better conformance with U.S. practice. New claims 10-20 have been added to

provide a fuller scope of coverage. Non-elected claims 3-6 have been canceled without prejudice or admission and subject to applicants' right to file a continuing application to pursue the subject matter of the non-elected claims.

Submitted herewith are replacement sheets for Figs. 8A-8B incorporating revisions to label sprocket halls 40 described on page 14 of the specification.

In view of the foregoing, applicants respectfully request that the objections to the abstract and claims 1 and 7 have been overcome and should be withdrawn.

Applicants request reconsideration of their application in light of the following discussion.

Summary of the Invention

The present invention is directed to a semiconductor device and to an electronic device equipped with the semiconductor device.

As described in the specification (pgs. 1-5), conventional semiconductor devices having flexible printed circuits and connection terminals suffer from poor connection and operational reliability and are expensive to manufacture.

The present invention overcomes the drawbacks of the conventional art. Figs. 7 and 8A show an embodiment of a semiconductor device according to the present invention embodied in the claims. The semiconductor device has a

flexible printed circuit on which a semiconductor chip is mounted. A connection terminal portion comprises connection terminal lands 15 arranged on the flexible printed circuit in one of a stepped configuration (e.g., see each of the single columns of connection terminal lands 15 in Fig. 7) and a grid configuration (e.g., see rows and columns of connection terminal lands 15 in Fig. 8A). Wirings 17 connect the respective connection terminal lands 15 to the semiconductor chip. An insulating film 16 is disposed on the wirings 17 but is not disposed on the connection terminal lands 15.

By the foregoing construction of the semiconductor device according to the present invention, by arranging the connection terminal lands on the flexible printed circuit in one of a stepped configuration and a grid configuration, and by disposing the insulating film on the wirings but not on the connection terminal lands, the connection and operational reliability of the semiconductor device is improved as compared to the conventional art.

Traversal of Prior Art Rejection

Claims 1, 2 and 7-9 were rejected under 35 U.S.C. §102(b) as being anticipated by Morishita. Applicants respectfully traverse this rejection and submit that amended claims 1, 2 and 7-9 recite subject matter which is not identically disclosed or described in Morishita.

Amended independent claim 1 is directed to a semiconductor device and requires a flexible printed circuit, a semiconductor chip mounted on the flexible printed circuit, a connection terminal portion comprising a plurality of connection terminal lands arranged on the flexible printed circuit in one of a stepped configuration and a grid configuration, a plurality of wirings connecting the respective connection terminal lands to the semiconductor chip, and an insulating film disposed on the wirings but not disposed on the connection terminal lands. No corresponding structural combination is disclosed or described by the prior art of record.

Morishita discloses a semiconductor device having a flexible printed circuit including connection terminal lands 8b (FPC electrodes), LSI electrodes 8a, and wirings 8 (input lines) connecting the connection terminal lands 8b to the respective LSI electrodes 8a (Figs. 1-3). An insulating film 7 is disposed on the wirings 8, the connection terminal lands 8b, and the LSI electrodes.

In contrast, amended independent claim 1 requires connection terminal lands arranged on a flexible printed circuit in one of a stepped configuration and a grid configuration. As shown in Fig. 1 of Morishita, the connection terminal lands 8b are arranged in a single column and in alignment with one another. Stated otherwise, the

connection terminal lands 8b do not form a stepped configuration. Furthermore, the single column of connection terminal lands 8b in Morishita does not define a grid configuration which requires, for example, a network of columns and rows.

Moreover, Morishita does not disclose or describe an insulating film disposed on the wirings but not disposed on the connection terminal lands. As shown in Fig. 2 of Morishita, the insulating film 7 is disposed on connection terminal lands 8b.

Amended independent claim 7 is directed to an electronic device and requires a connection terminal portion comprising a plurality of connection terminal lands arranged on the flexible printed circuit in one of a stepped configuration and a grid configuration. No corresponding structure is disclosed or described by Morishita as set forth above for amended independent claim 1.

In the absence of the foregoing disclosure recited in amended independent claims 1 and 7, anticipation cannot be found. See, e.g., W.L. Gore & Associates v. Garlock, Inc., 220 USPQ 303, 313 (Fed. Cir. 1983), cert. denied, 469 U.S. 851 (1984) ("Anticipation requires the disclosure in a single prior art reference of each element of the claim under consideration"); Continental Can Co. USA v. Monsanto Co., 20 USPQ2d 1746, 1748 (Fed. Cir. 1991) ("When more than one

reference is required to establish unpatentability of the claimed invention anticipation under § 102 can not be found".); Lindemann Maschinenfabrik GmbH v. American Hoist & Derrick Co., 221 USPQ 481, 485 (Fed. Cir. 1984) (emphasis added) ("Anticipation requires the presence in a single prior art reference disclosure of each and every element of the claimed invention, arranged as in the claim").

Stated otherwise, there must be no difference between the claimed invention and the reference disclosure, as viewed by a person of ordinary skill in the field of the invention. This standard is clearly not satisfied by Morishita for the reasons stated above. Furthermore, Morishita does not suggest the claimed subject matter and, therefore, would not have motivated one skilled in the art to modify Morishita's semiconductor device to arrive at the claimed invention.

Claims 2 and 8-9 depend on and contain all of the limitations of amended independent claims 1 and 7, respectively, and, therefore, distinguish from Morishita at least in the same manner as claims 1 and 7.

In view of the foregoing, applicants respectfully request that the rejection of claims 1, 2 and 7-9 under 35 U.S.C. §102(e) as being anticipated by Morishita be withdrawn.

Applicants respectfully submit that new claims 10-20 also patentably distinguish from the prior art of record.

New independent claim 10 is directed to a semiconductor device and requires a plurality of rows and columns of connection terminal lands arranged on a flexible printed circuit, a plurality of wirings connecting the respective connection terminal lands to a semiconductor chip, and an insulating film disposed on the wirings but not disposed on the connection terminal lands. No corresponding structural combination is disclosed or suggested by the prior art of record as set forth above for amended independent claim 1.

Claims 11-20 depend on and contain all of the limitations of independent claim 10 and, therefore, distinguish from the prior art of record at least in the same manner as claim 10.

In view of the foregoing amendments and discussions, the application is now believed to be in allowable form. Accordingly, favorable reconsideration and passage of the application to issue are most respectfully requested.

Respectfully submitted,

ADAMS & WILKS
Attorneys for Applicants

By _____
Bruce L. Adams
Reg. No. 25,386

50 Broadway - 31st Floor
New York, NY 10004
(212) 809-3700

MAILING CERTIFICATE

I hereby certify that this correspondence is being deposited with the United States Postal Service as first-class mail in an envelope addressed to: MS FEE AMENDMENT, COMMISSIONER FOR PATENTS, P.O. Box 1450, Alexandria, VA 22313-1450, on the date indicated below.

Debra Buonincontri
Name

Debra Buonincontri
Signature

May 3, 2005
Date

IN THE DRAWINGS:

Submitted herewith are replacement sheets for Figs. 8A-8B incorporating revisions to label sprocket halls 40.